Sierra Components, Inc.

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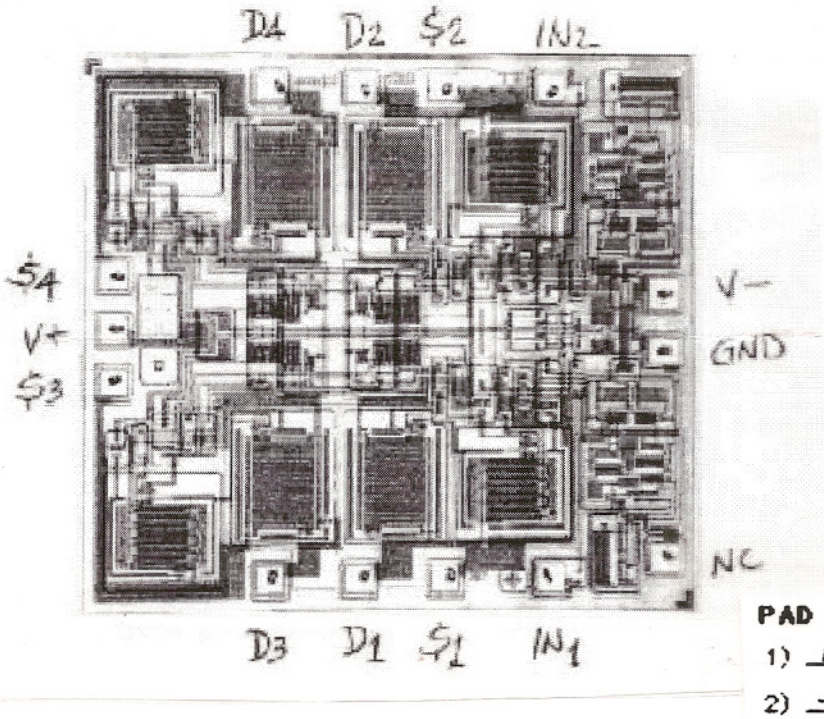
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



PAD FUNCTIONS

1)	NC	10)	$2
2)	$3	11)	D2
3)	D3	12)	D4
4)	D1	13)	$4
5)	$1	14)	V+
6)	IN1	15)	
7)	GND	16)	
8)	V-	17)	
9)	IN2	18)	

Topside Metal: Al
Backside: Si
Backside Potential:
Mask Ref:
Bond Pads : .004" min

APPROVED BY: CD	**DIE SIZE : .076" x .083"**	**DATE: 2/5/01**
MFG: Harris	**THICKNESS: .020"**	**P/N: HI307-2**